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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/21/2001

Niels Christian Finseth

42390.P11872

3452

7590

09/01/2006

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EXAMINER

BURD, KEVIN MICHAEL

ART UNIT

PAPER NUMBER

2611

DATE MAILED: 09/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/856,807

Applicant(s)

FINSETH, NIELS CHRISTIAN

Examiner

Kevin M. Burd

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 14 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 13-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 13-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

1. This office action, in response to the request for continued examination (RCE) and amendment filed 8/14/2006, is a non-final office action.

***Continued Examination Under 37 CFR 1.114***

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/14/2006 has been entered.

***Response to Arguments***

3. Applicant's arguments with respect to claims 13-31 have been considered but are moot in view of the new ground of rejection.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 13-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuyoshi et al (US 4,949,325) in view of Huber (US 4,110,557) further in view of Inada et al (US 5,534,807).

Regarding claims 13, 19, 20 and 26, Tsuyoshi discloses a method and circuit for recovering a data signal and a clock signal in figure 5. A signal (S1) is received and a data signal (17) and a clock signal (S4) are generated. The data signal and the clock signal (the output of element 19) are phase locked by measuring the phase difference (36). The phase compare delays the signal in element 19 and the delayed clock is input to the data demodulator 18 to generate the READOUT DATA. Tsuyoshi does not disclose the clock signal is generated from a resonator circuit. Tsuyoshi discloses using a VCO 15 in the PLL circuit that generates the clock signal from the input signal (S1). Crystal resonators are commonly used in these circuits and it would have been obvious for one of ordinary skill in the art at the time of the invention to utilize a simple and readily available clock circuit for the oscillator. Tsuyoshi does not disclose delaying the received data signal to compensate for a delay created in the generating of the clock signal so that the data signal is synchronized with the clock signal. Huber discloses means to delay transmission of the data signal to the phase and frequency detector to synchronize the data signal with the clocking signal received from the frequency divider (column 6, lines 46-50). The circuitry is shown in figure 2. It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the means for delaying the data signal of Huber into the method and circuit for recovering a data signal and a clock signal of Tsuyoshi. This synchronization will reduce the error detected in the

Art Unit: 2611

phase detector and allow for smaller adjustments to occur, allowing the data and clock signals to be locked. The combination of Tsuyoshi and Huber does not disclose the measuring of a phase difference includes sampling the data signal with the clock signal in three flip-flops at three different points in time. Inada discloses a phase difference detecting circuit shown in figure 2. The circuit includes sampling the data signal (DI) with a clock signal (CLK) in three flip-flops (6b, 6c and 6d) at three different points in time (column 12, lines 4-8) shown in figure 4. These sampled signals are input to the phase difference determining circuit 5. It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the phase difference detecting circuit of Inada into the circuit and method of using the circuit of the combination of Tsuyoshi and Huber. Flip-flops are inexpensive components and using them to sample and determine a phase difference will reduce the cost of the circuit.

Regarding claims 14, 21 and 27, Tsuyoshi discloses generating a signal output from the phase compare 36. This signal controls the delay element 19.

Regarding claims 15, 22 and 28, Tsuyoshi discloses generating a signal based in the frequency difference (13) of an input clock and the clock (S4).

Regarding claims 16-18, 23-25 and 29-31, Tsuyoshi discloses filtering the input to the VCO 15 in figure 5.

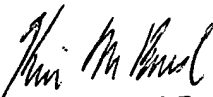
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Friday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kevin M. Burd  
8/17/2006

  
**KEVIN BURD**  
**PRIMARY EXAMINER**